REMARKS/ARGUMENTS

The Office Action mailed April 8, 2005 has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Claim Status and Amendment to the Claims

Claims 1-13 are now pending.

Claims 1, 5, 7 and 9 have been amended to further particularly point out and distinctly claim subject matter regarded as the invention. Support for these changes may be found in the specification, page 7, lines 4-15, page 10, line 14 to page 11, line16, and FIG. 4, for example. The amendment also contains minor changes of a clerical nature.

The text of claims 2-4, 6, and 8 is unchanged, but their meaning is changed because they depend from amended claims.

New claims 10-13 has been added, which also particularly point out and distinctly claim subject matter regarded as the invention. Claim 12 is a method claim corresponding to claim 1.

No "new matter" has been added by the amendment.

Election/Restriction Requirement

The Examiner is thanked for his kind withdrawal of the restriction requirement made in the Office action mailed on March 24, 2004.

The 35 U.S.C. §102 Rejection

Claims 1-9 stand rejected under 35 U.S.C. §102(e) as being allegedly anticipated

by Inagaki (U.S. Pat. No. 6,421,773), among which claims 1 and 9 are independent claims. This rejection is respectfully traversed.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 869 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). *See also*, M.P.E.P. §2131.

In the Office Action, the Examiner alleges that the elements of the presently claimed invention are disclosed in *Inagaki*, and specifically contends that *Inagaki*'s "program counter controller handles a content of the program counter, that is, the value showing an address to be read next in the instruction memory, through increment (n+1), decrement or hold operation, and loads the value to the program counter," citing Figures 1 and 2, column 2 lines 20-52 column 7 lines 11-293 [sic] of *Inagaki*. The Applicants respectfully disagree for the reasons set forth below.

Claim 1 defines a sequence control circuit which comprises a program counter control section and an instruction memory section. The claimed program counter control section decodes, in an n-th clock cycle, a sequence control instruction that is executed in the n-th clock cycle, determines, in the n-th clock cycle, a program counter signal for specifying a sequence control instruction to be executed in an (n+1)th clock cycle, and

outputs, in the (n+1)th cycle, the determined program counter signal as an instruction memory address, as recited in Claim 1 as amended. Furthermore, the claimed instruction memory section reads, in the n-th cycle, said sequence control instruction to be executed in the (n+1)th clock cycle based on a program counter signal for specifying said sequence control instruction that is executed in the n-th clock cycle, and outputs, in the (n+1)th clock cycle, the read sequence control instruction to said program counter control section, as recited in Claim 1 as amended. Claims 9 and 12 also include substantially the same distinctive feature as claim 1.

Accordingly, in accordance with the claimed invention, the sequence control instruction which is to be decoded and executed in the (n+1)th clock cycle (for example, clock cycle t2) is read from the instruction memory section in the n-th clock cycle (for example, clock cycle t1), i.e., just one cycle before its decoding and execution in the (n+1)th clock cycle. The thus read sequence control instruction is supplied to the program counter control section in the (n+1)th clock cycle, i.e., just one cycle after its reading in the n-th clock cycle. In addition, the program counter signal specifying a sequence control instruction to be executed in the (n+1)th lock cycle is determined by decoding the sequence control instruction executed in the n-th clock cycle, that is, one cycle before the (n+1)th clock cycle. Thus determined program counter signal is supplied to the instruction memory section as an instruction memory address in the (n+1)th clock cycle, that is, just one cycle after its determination in the n-th clock cycle.

Thus, in accordance with the claimed invention, reading a sequence control instruction is performed in a first clock cycle (for example, t1), and decoding and execution of the sequence control signal is performed in the next (second) clock cycle (for example, t2) which is different from the first clock cycle. In addition, determining the program counter signal specifying a sequence control instruction to be executed in a next clock cycle (for example, t2) is performed in a previous clock cycle (for example, t1), and then, in the next clock cycle (t2), the sequence control signal is read from the instruction memory section and executed. By performing these operations in different clock cycles, the maximum speed of operation of the sequence control circuit is determined by either an access time of the instruction memory section or a processing time corresponding to the speed of operation of the program counter control section, more specifically, by the larger of the two.

On the other hand, *Inagaki* performs a series of operations including the reading of instruction memory **21/121**, the determination of the value of a program counter, and the setting of the program counter, in a single clock cycle. That is, *Inagaki* merely discloses a conventional sequence control circuit similar to that explained in the Description of the Related Art of the present specification (page 4, lines 16-23). Therefore, the maximum speed of operation of the sequence control circuit of *Inagaki* is determined by a sum of an access time of the instruction memory **21/121** and the processing time corresponding to the speed of operation of the program counter control section **24/124**.

It should be noted that the content of the program counter **122** of *Inagaki* indicates the address in the instruction memory **121** (see column 2, lines 47-51 thereof). That is, *Inagaki*'s "inclement" is that for memory address and not for the clock cycle as the Examiner alleges. Thus, although *Inagaki* may describe a program counter controller for controlling the program counter according to a control word read form the instruction memory (column 4, lines 8-10 and column 7, lines 21-23 thereof), *Inagaki*'s operations are performed within a single clock cycle in the same manner as a conventional sequence control circuit, as discussed above.

Accordingly, *Inagaki* does not disclose or teach the program counter control section of the claimed invention. It is respectfully requested that the rejection of claims based on *Inagaki* be withdrawn. In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Dependent Claims

Claims 2-8 and 10 depend from claim 1, claim 11 depends from claim 9, and claim 13 depends from claim 12, and thus include the limitations of claims 1, 9, and 12, respectively. The argument set forth above is equally applicable here. The base claims being allowable, the dependent claims must also be allowable at least for the same reasons.

Conclusion

It is believed that this Amendment places the above-identified patent application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-1698.

Respectfully submitted,
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